



PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the application of:
Ryan Fung

Application No.: 10/774,857

Filed: February 9, 2004

Title: Method and Apparatus For Utilizing Long-
Path and Short-Path Timing Constraints In
An EDA Tool for Routing

Attorney Docket No. ALT.P027.1 (A1182.1)

Examiner: Tat, Binh C

Art Unit: 2825

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Dear Sir:

This Information Disclosure Statement is believed to be filed before the mailing date of a final office action on the merits under 37 CFR §1.97(c). The fee of \$180 set forth in 37 CFR §1.17(p) is being submitted herewith. If it is determined that any additional fees are due, the Commissioner is hereby authorized to charge such fees to Deposit Account 50-1624.

The references listed in the attached PTO Form PTO/SB/08A and 08B, may be material to examination of the above-identified patent application. Applicant submits these references in compliance with his duty of disclosure pursuant to 37 CFR §§1.56 and 1.97. The Examiner is requested to make these references of official record in this application.

CERTIFICATE OF MAILING

Date of Deposit May 19, 2006

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date indicated above.

Lawrence M. Cho

(Typed or printed name of person mailing correspondence)

L.M.Cho

(Signature of person mailing correspondence)

This Information Disclosure Statement is not to be construed as a representation that a search has been made, that additional information material to the examination of this application does not exist, or that these references indeed constitute prior art.

If there are any additional charges, please charge them to Deposit Account No. 50-1624.

Respectfully submitted,

Dated: May 19, 2006

P.O. Box 2144
Champaign, IL 61825
Tel: (217) 377-2500
Fax: (217) 356-7373



Lawrence M. Cho
Attorney for Applicant
Reg. No. 39,942

MAY 22 2006

PTO/SB/08A (07-05)

Approved for use through 07/31/2006. OMB 0651-0031
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Substitute for form 1469 PTO

PATENT TRADEMARK

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 1

of 2

Complete if Known

Application Number	10/774,857
Filing Date	February 9, 2004
First Named Inventor	Ryan Fung
Art Unit	2825
Examiner Name	Tat, Binh C
Attorney Docket Number	ALT.P027.1 (A1182.1)

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number Number-Kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US- 6,826,773	11-2004	Hathaway et al.	
		US- 6,763,506	07-2004	Betz et al.	
		US- 6,708,139	03-2004	Rearick et al.	
		US- 5,659,484	08-1997	Bennett et al.	
		US- 5,541,849	07-1996	Rostoker et al.	
		US- 5,237,514	08-1993	Curtin, James J.	
		US- 5,521,837	05-1996	Frankle et al.	
		US- 2005/0251775	11-2005	Wood, John	
		US- 2005/0138578	06-2005	Alpert et al.	
		US- 2005/0132318	06-2005	Kidd et al.	
		US- 2005/0039156	02-2005	Catthoor et al.	
		US- 2004/0243964	12-2004	McElvain et al.	
		US- 2003/0005398	01-2003	Cho et al.	
		US-			

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Foreign Patent Document Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T ⁶

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STATEMENT BY APPLICANT**

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Sheet

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of

2

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First Named Inventor	Ryan Fung
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Examiner Name	Tat, Binh C

Attorney Docket Number

ALT.P027.1 (A1182.1)

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		NN9107410, "Linear Algorithm for Distributing Slack So That All Nets of a Design Have a Zero Slack Pin", IBM Technical Disclosure Bulletin, Vol. 34, No. 2, July 1991, pp. 410-414.	
		Mathur et al., "Timing-Driven Placement for Regular Architectures", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 16, No. 6, June 1997, pp. 597-608.	

Examiner Signature	Date Considered
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